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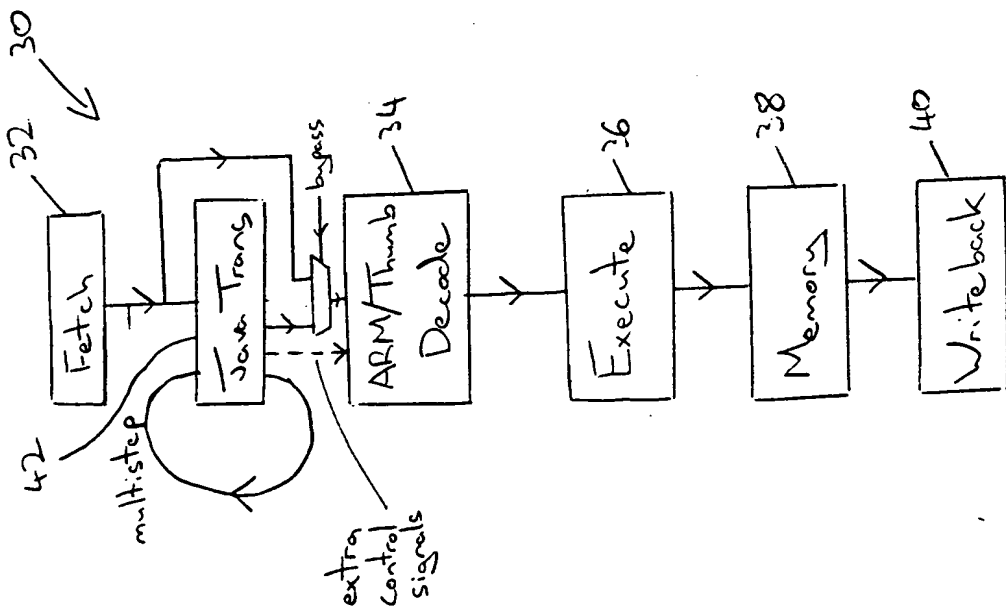


Fig. 1

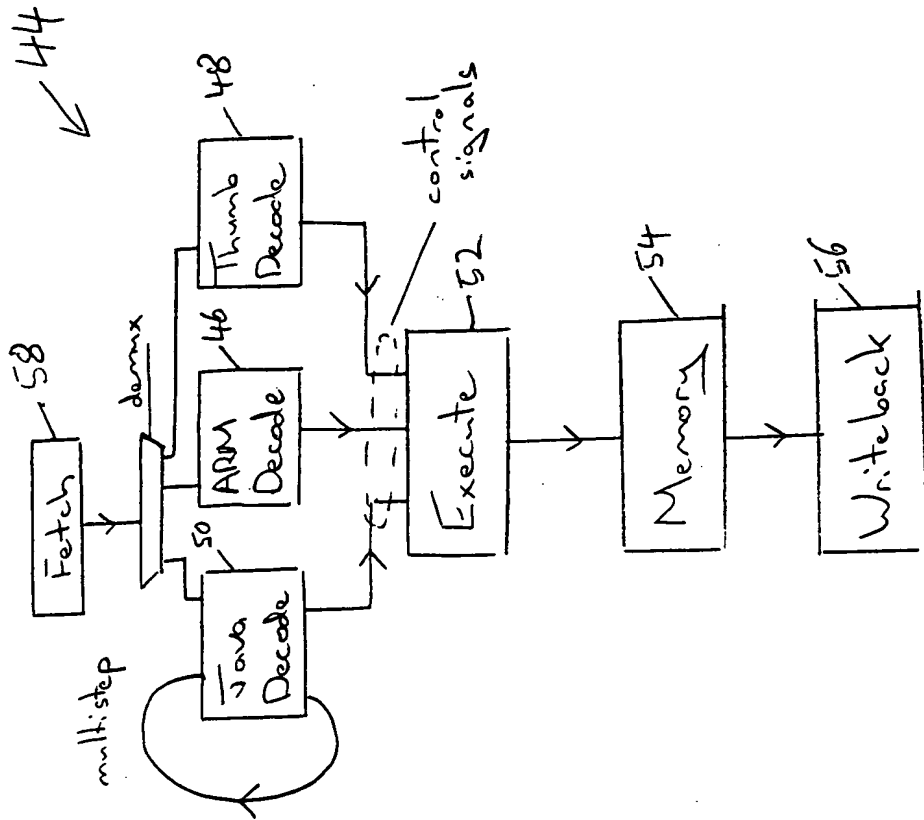


Fig. 2

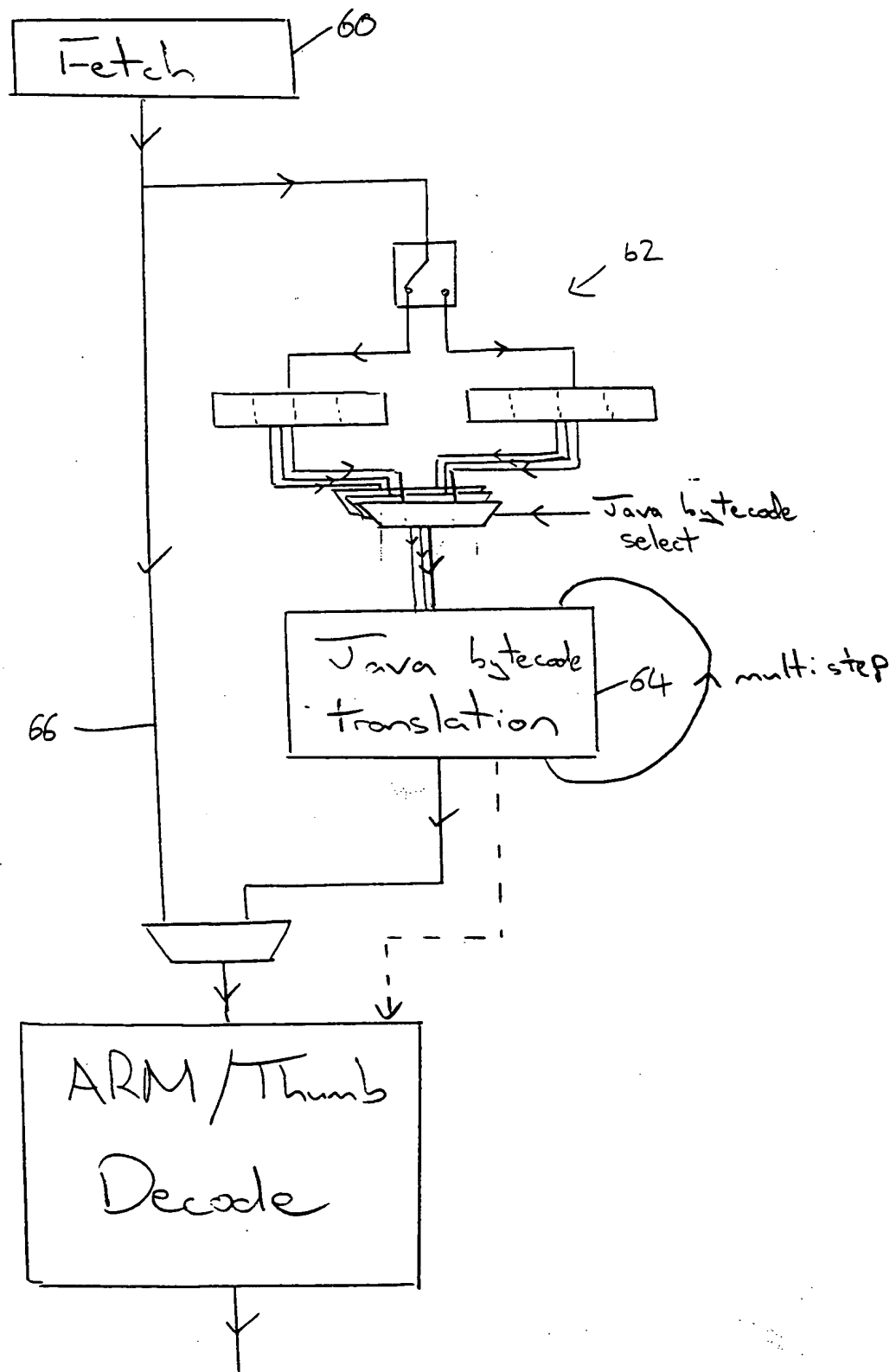


Fig. 3

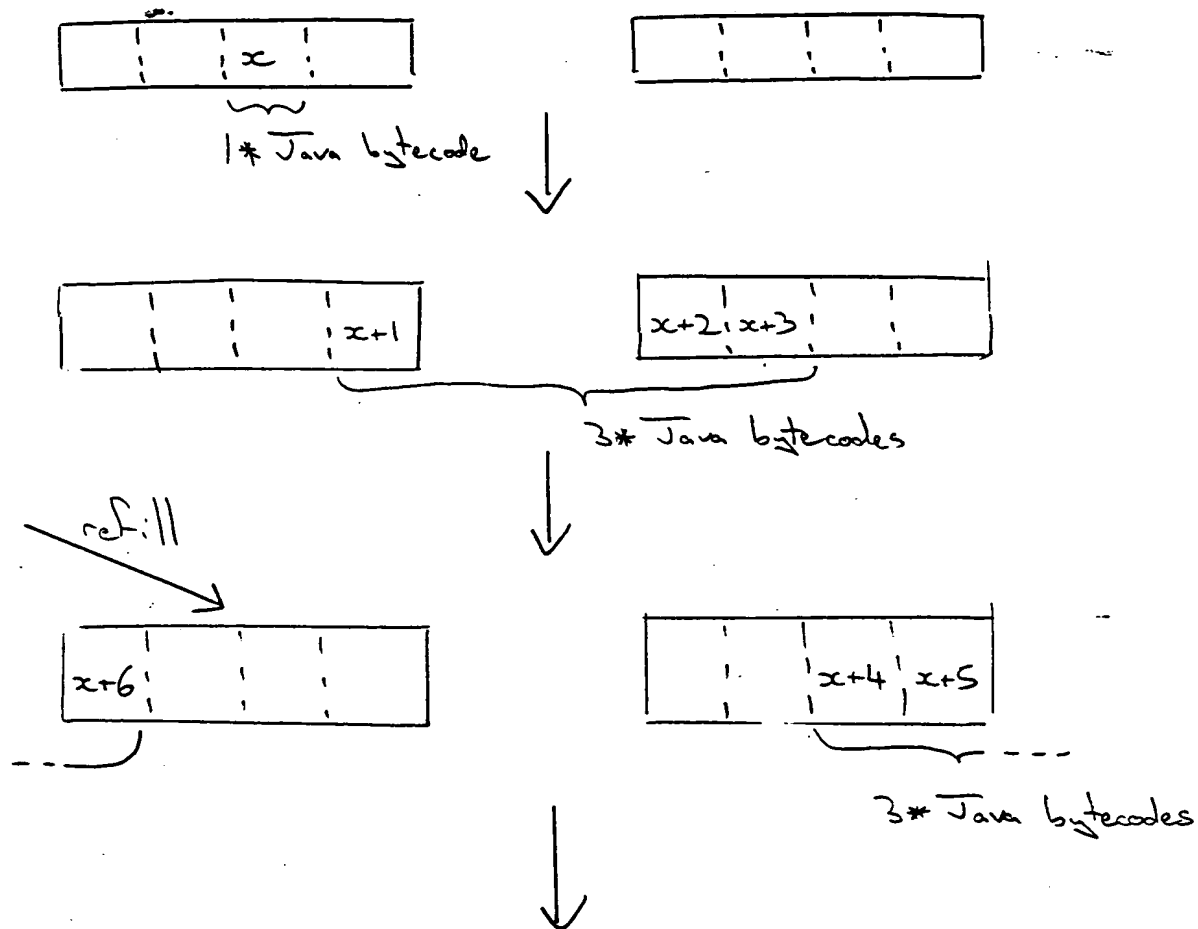


Fig. 4

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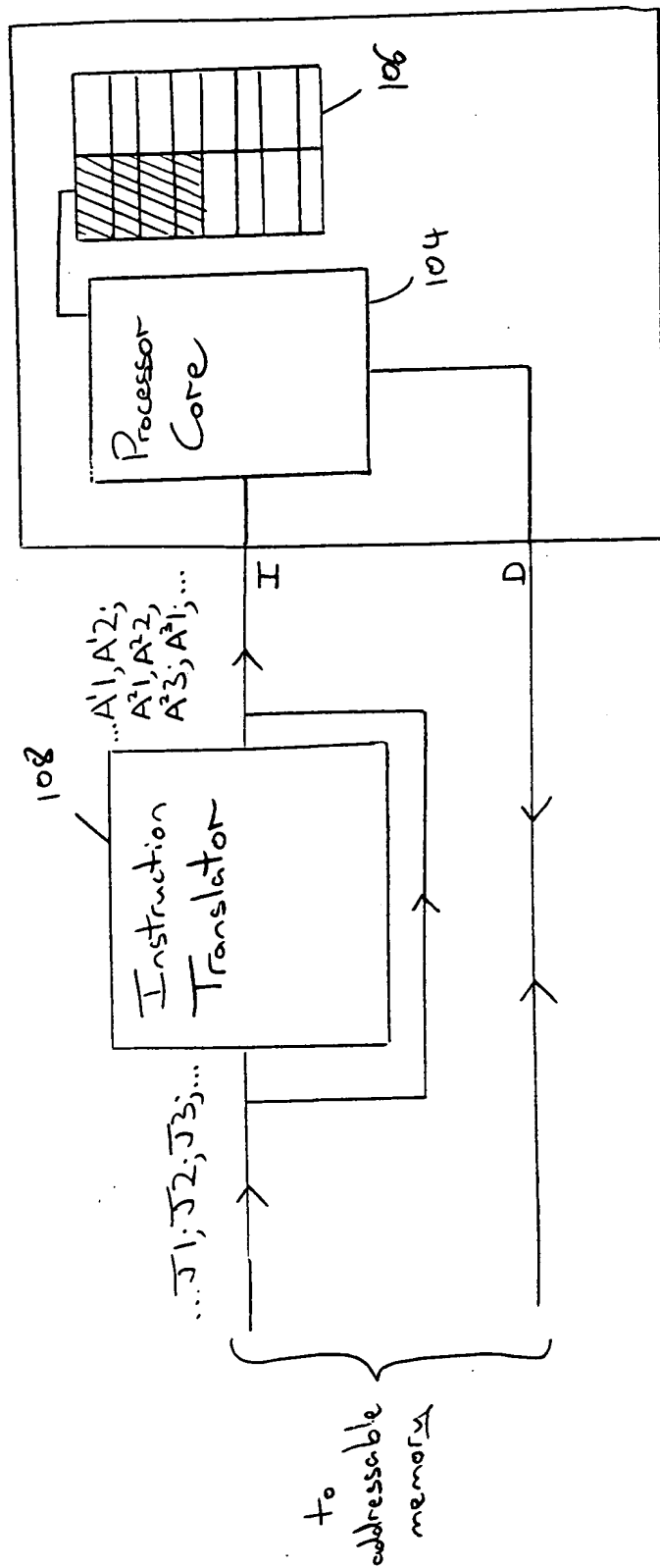


Fig. 5

Fig. 6

Java Instruction	load (RF=2, RF>0)	load (RF=2, RF>1)	load (SA=-1)
ARM Instruction(s)	\nearrow LDR R0[Rstack, #4]! (POP)	LDR R3[Rstack, #4]! (POP)	ADD R3, R3, R0 \nearrow
State	0000	00100	01000
R0	E	SOA TOS	SOA TOS
R1	E	E	E
R2	E	E	E
R3	E	E	(SOA+SOB) TOS

Java Instruction	load (RF=0, RE=2)	load^2 (RF=0, RE>2)	load^2 (RF=0, RE=2)
ARM Instructions	\nearrow LDR R1, [Rvars, #4] LDR R0, [Rvars, #0]	\nearrow STR R3[Rstack, #4] (PUSH)	LDR R3, [Rvars, #4] LDR R2, [Rvars, #0]
State	0011	01101	01001
R0	E	SOA TOS-1	SOA TOS-1
R1	E	SOA TOS	SOA TOS-2
R2	E	E	SOA TOS-1
R3	(SOA+SOB) TOS	(SOA+SOB) TOS-2	SOA TOS

load
 RF=2 SA=0
 RE=2 (swap)

01001

Array Ref	TOS-1
Index	TOS
	E
	E

LDR R12, [R0, #0]
 LDR R2, [R12, R1, LSL #3]!

01001

Array Ref	TOS-1
Index	TOS
1st Array Word	E
	E

01011

Array Ref	E
Index	E
1st Array Word	TOS-1
2nd Array Word	TOS

LDR R3, [R12, #4]
 (state swap)

Fig. 7

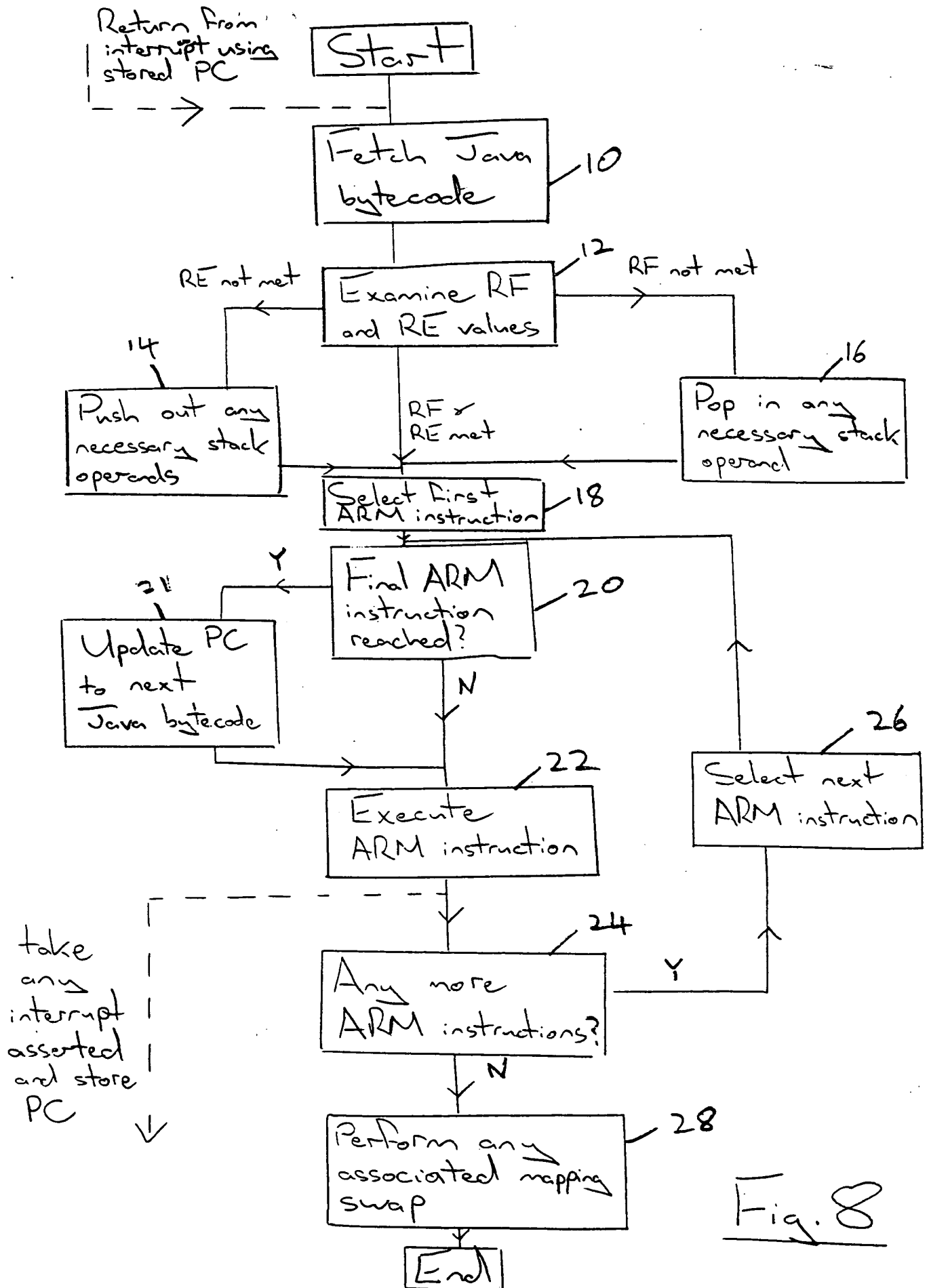


Fig. 8

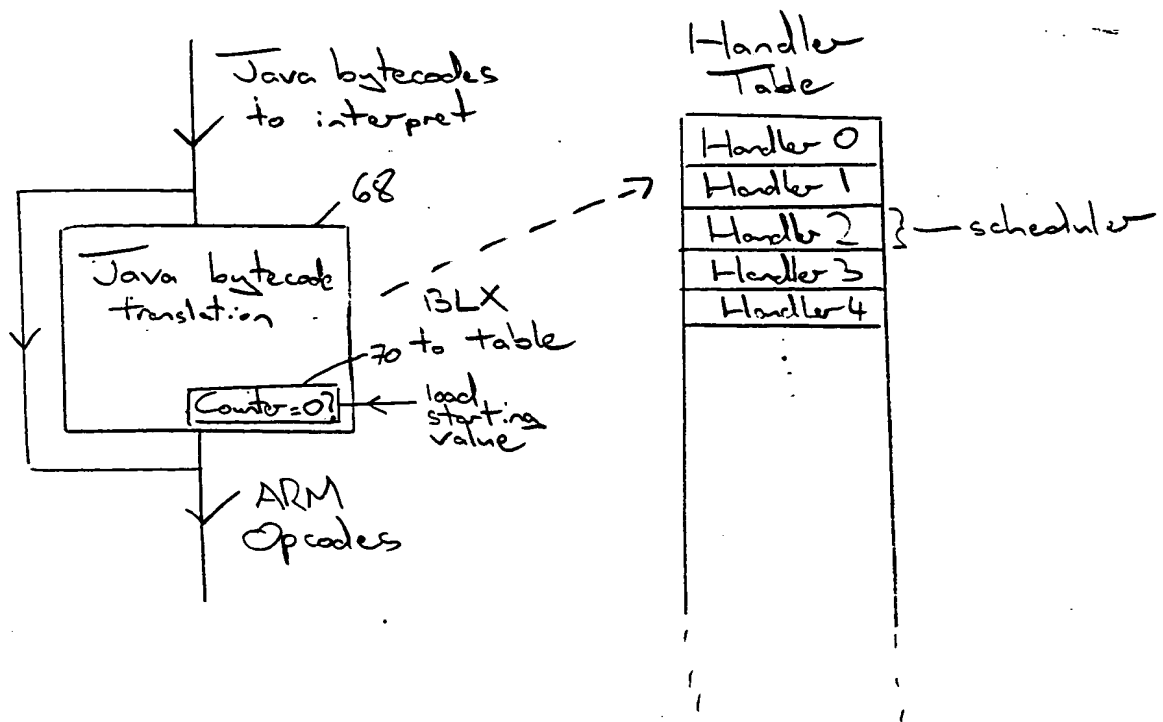


Fig. 9

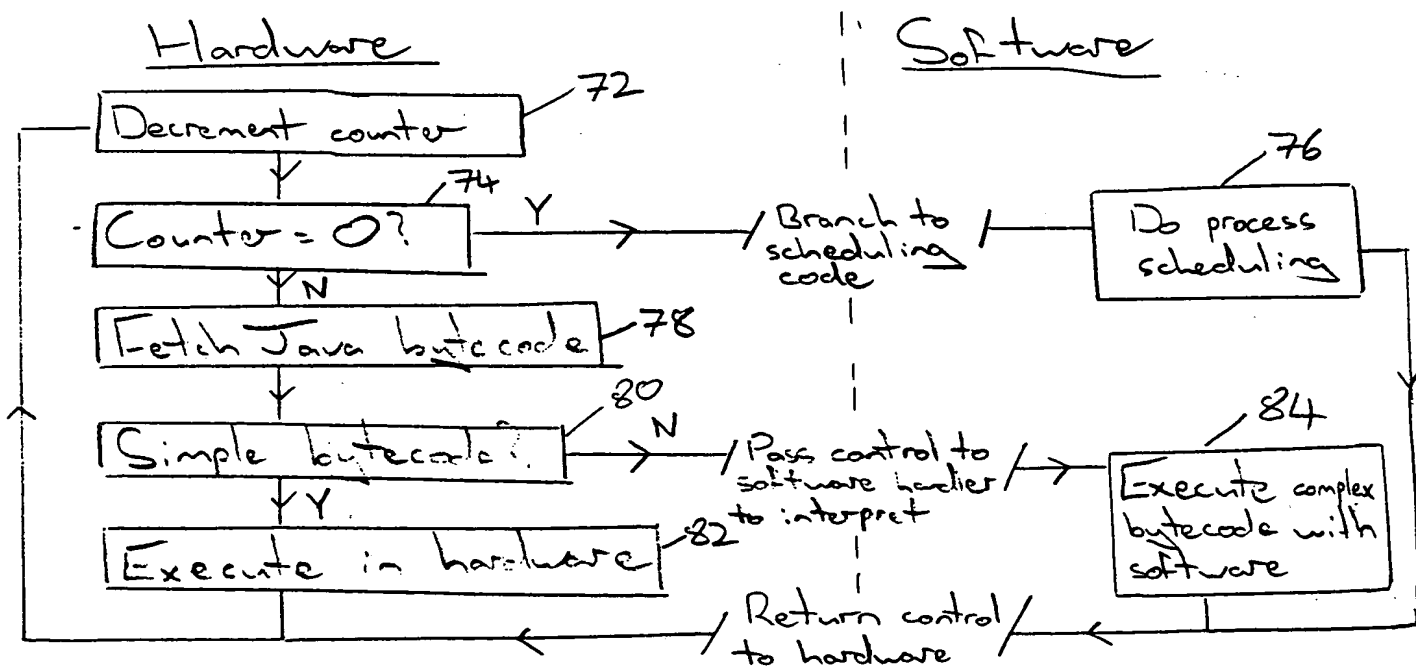


Fig. 10

Hardware

Software

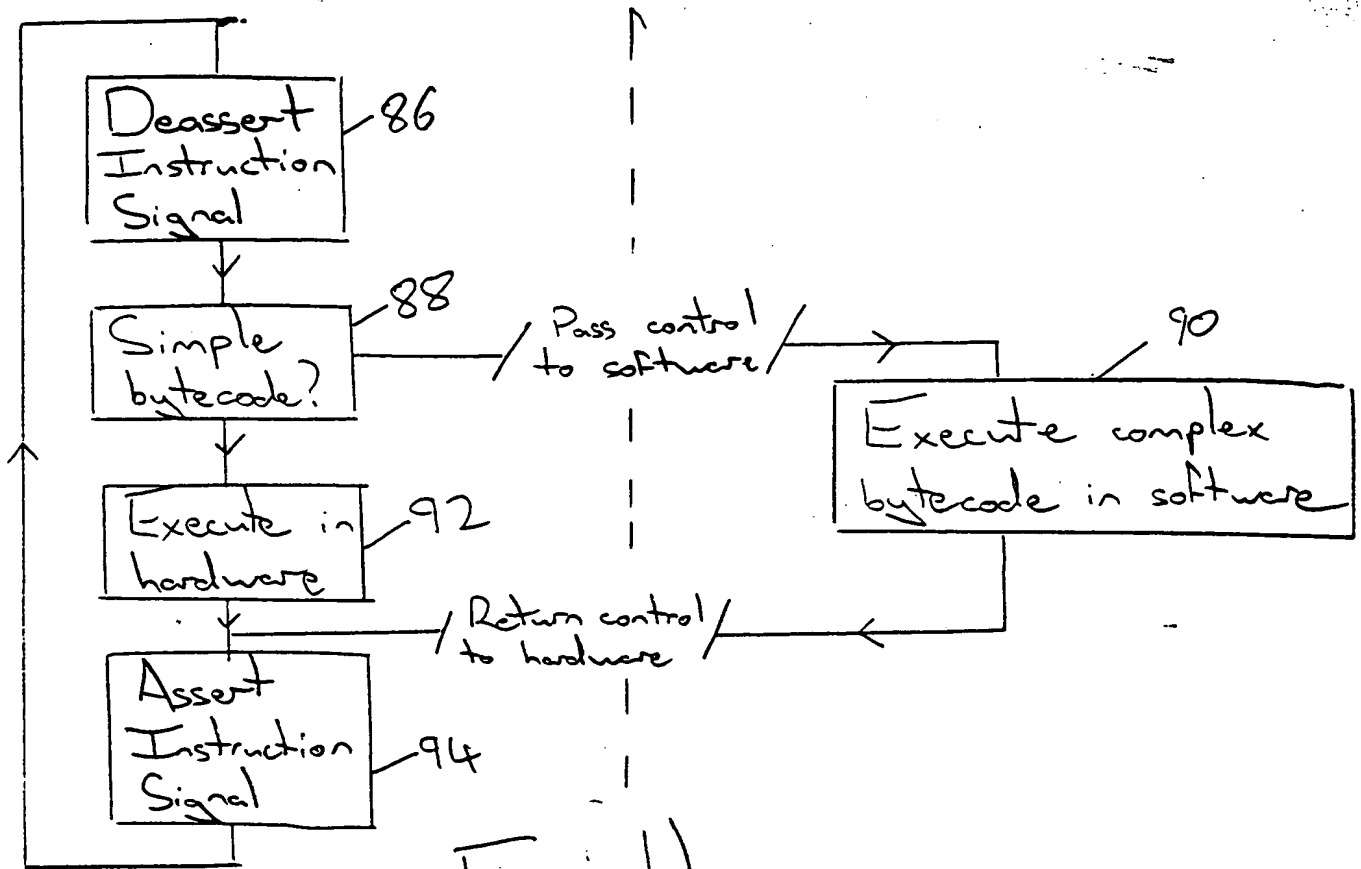


Fig. 11

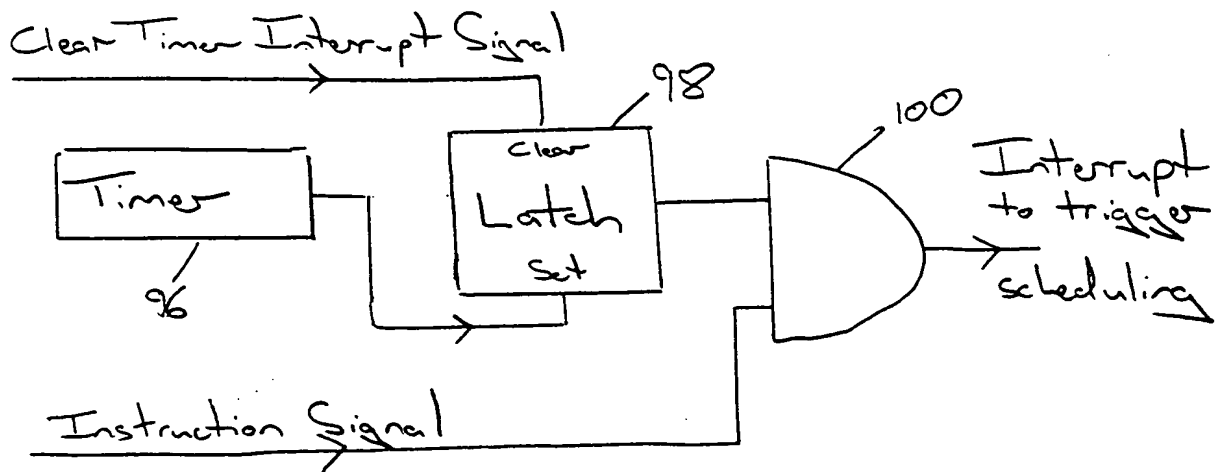


Fig. 12

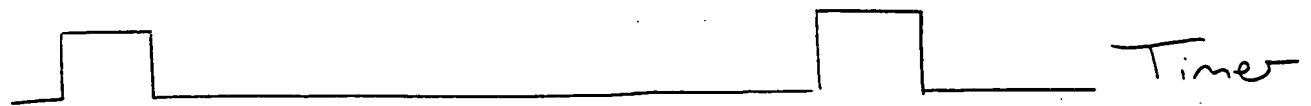
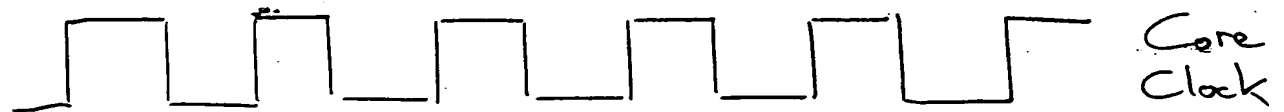


Fig. 13